ABSTRACT:

A simple and cost-effective method to improve ESD performance by selectively reducing avalanche breakdown voltage in protection devices by means of locally increasing the acceptor dopant concentration.

The present invention relates to an integrated circuit arrangement and method of forming on a semiconductor substrate an electrostatic discharge (ESD) protecting device together with internal circuitry to be protected by said protecting device, wherein an offset transistor arrangement is formed in said protecting device, and an acceptor concentration is increased at said offset transistor arrangement so as to selectively reduce the breakdown voltage of the offset transistor arrangement. The lower breakdown voltage causes the protection devices to trigger at lower voltage during an ESD event, thus protecting the more vulnerable regular LDD transistors.

Fig. 4B